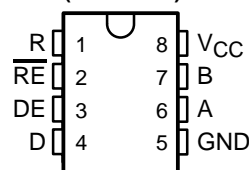


# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

- Bidirectional Transceivers
- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . .  $\pm 60$  mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 k $\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From Single 5-V Supply

SN65176B . . . D OR P PACKAGE  
SN75176B . . . D, P, OR PS PACKAGE  
(TOP VIEW)



## description/ordering information

The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	SN75176BP	SN75176BP
	SOIC (D)	Tube of 75	SN75176BD	75176B
		Reel of 2500	SN75176BDR	
SOP (PS)	Reel of 2000	SN75176BPSR	A176B	
-40°C to 105°C	PDIP (P)	Tube of 50	SN65176BP	SN65176BP
	SOIC (D)	Tube of 75	SN65176BD	65176B
		Reel of 2500	SN65176BDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## description/ordering information (continued)

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

### Function Tables

#### DRIVER

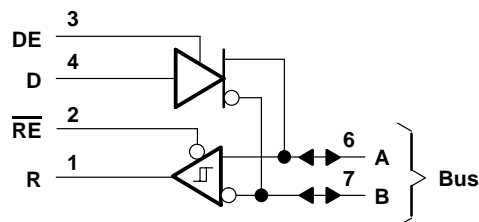
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

#### RECEIVER

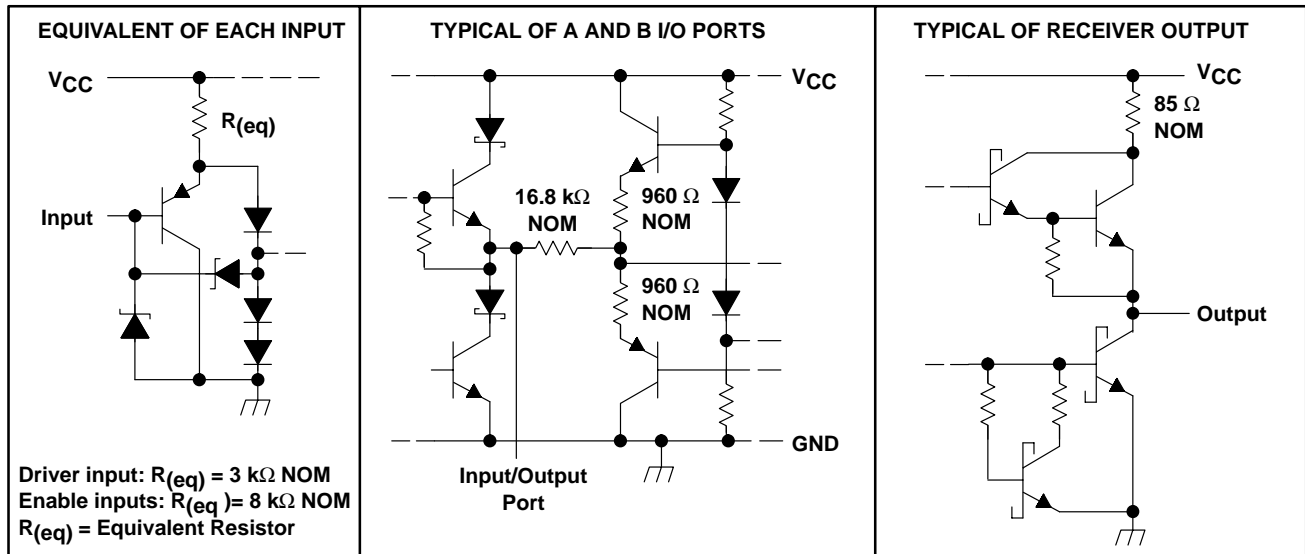
DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

### logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Enable input voltage, $V_I$	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	
D package	97°C/W
P package	85°C/W
PS package	95°C/W
Operating virtual junction temperature, $T_J$	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
  2. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A) / \theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## recommended operating conditions

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (separately or common mode)			12	V
				-7	
V <sub>IH</sub>	High-level input voltage	D, DE, and $\overline{RE}$		2	V
V <sub>IL</sub>	Low-level input voltage	D, DE, and $\overline{RE}$		0.8	V
V <sub>ID</sub>	Differential input voltage (see Note 4)			±12	V
I <sub>OH</sub>	High-level output current	Driver		-60	mA
		Receiver		-400	μA
I <sub>OL</sub>	Low-level output current	Driver		60	mA
		Receiver		8	
T <sub>A</sub>	Operating free-air temperature	SN65176B		-40	°C
		SN75176B		0	

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal A, with respect to the inverting terminal B.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V
V <sub>O</sub>	Output voltage	I <sub>O</sub> = 0		0		6	V
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0		1.5	3.6	6	V
V <sub>OD2</sub>	Differential output voltage	R <sub>L</sub> = 100 Ω,	See Figure 1	1/2 V <sub>OD1</sub> or 2 V††			V
		R <sub>L</sub> = 54 Ω,	See Figure 1	1.5	2.5	5	
V <sub>OD3</sub>	Differential output voltage	See Note 5		1.5		5	V
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage§	R <sub>L</sub> = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V <sub>OC</sub>	Common-mode output voltage	R <sub>L</sub> = 54 Ω or 100 Ω,	See Figure 1			+3 -1	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage§	R <sub>L</sub> = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
I <sub>O</sub>	Output current	Output disabled, See Note 6	V <sub>O</sub> = 12 V			1	mA
			V <sub>O</sub> = -7 V			-0.8	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 2.4 V				20	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.4 V				-400	μA
I <sub>OS</sub>	Short-circuit output current	V <sub>O</sub> = -7 V				-250	mA
		V <sub>O</sub> = 0				-150	
		V <sub>O</sub> = V <sub>CC</sub>				250	
		V <sub>O</sub> = 12 V				250	
I <sub>CC</sub>	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

§ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

†† The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

NOTES: 5. See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

6. This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics, V<sub>CC</sub> = 5 V, R<sub>L</sub> = 110 Ω, T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>d</sub> (OD)	Differential-output delay time	R <sub>L</sub> = 54 Ω,	See Figure 3		15	22	ns
t <sub>t</sub> (OD)	Differential-output transition time	R <sub>L</sub> = 54 Ω,	See Figure 3		20	30	ns
t <sub>PZH</sub>	Output enable time to high level	See Figure 4			85	120	ns
t <sub>PZL</sub>	Output enable time to low level	See Figure 5			40	60	ns
t <sub>PHZ</sub>	Output disable time from high level	See Figure 4			150	250	ns
t <sub>PLZ</sub>	Output disable time from low level	See Figure 5			20	30	ns

# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$V_O$	$V_{Oa}, V_{Ob}$	$V_{Oa}, V_{Ob}$
$ V_{OD1} $	$V_O$	$V_O$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		$V_t$ (test termination measurement 2)
$\Delta V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{Os} $	$ V_{Os} $
$\Delta V_{OC} $	$ V_{Os} - \bar{V}_{Os} $	$ V_{Os} - \bar{V}_{Os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$

## RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$V_O = 2.7 V,$	$I_O = -0.4 mA$			0.2	V
$V_{IT-}$	Negative-going input threshold voltage	$V_O = 0.5 V,$	$I_O = 8 mA$	$-0.2\ddagger$			V
$V_{hys}$	Input hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				50		mV
$V_{IK}$	Enable Input clamp voltage	$I_I = -18 mA$				-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 mV,$ See Figure 2	$I_{OH} = -400 \mu A,$		2.7		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 mV,$ See Figure 2	$I_{OL} = 8 mA,$			0.45	V
$I_{OZ}$	High-impedance-state output current	$V_O = 0.4 V$ to $2.4 V$				$\pm 20$	$\mu A$
$I_I$	Line input current	Other input = 0 V, See Note 7	$V_I = 12 V$			1	mA
			$V_I = -7 V$			-0.8	
$I_{IH}$	High-level enable input current	$V_{IH} = 2.7 V$				20	$\mu A$
$I_{IL}$	Low-level enable input current	$V_{IL} = 0.4 V$				-100	$\mu A$
$r_I$	Input resistance	$V_I = 12 V$			12		k $\Omega$
$I_{OS}$	Short-circuit output current			-15		-85	mA
$I_{CC}$	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at  $V_{CC} = 5 V, T_A = 25^\circ C.$

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 7: This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.



# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$ , See Figure 6		21	35	ns
$t_{PHL}$ Propagation delay time, high- to low-level output			23	35	
$t_{PZH}$ Output enable time to high level	See Figure 7		10	20	ns
$t_{PZL}$ Output enable time to low level			12	20	
$t_{PHZ}$ Output disable time from high level	See Figure 7		20	35	ns
$t_{PLZ}$ Output disable time from low level			17	25	

## PARAMETER MEASUREMENT INFORMATION

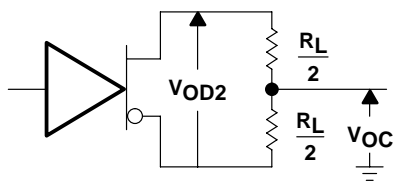


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

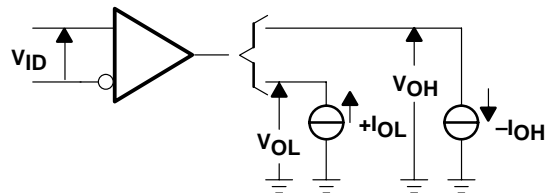
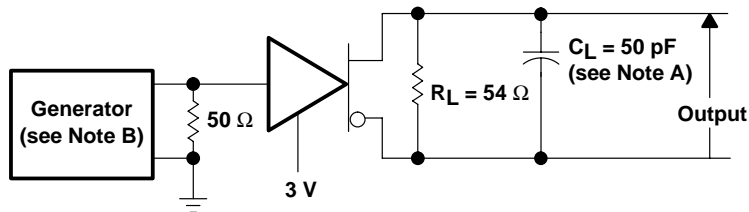
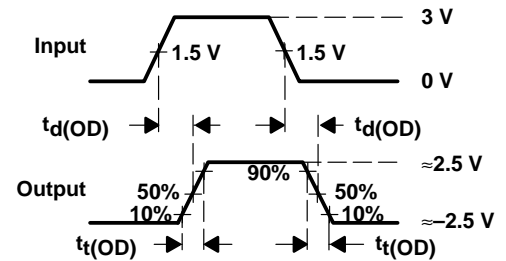


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$



TEST CIRCUIT



VOLTAGE WAVEFORMS

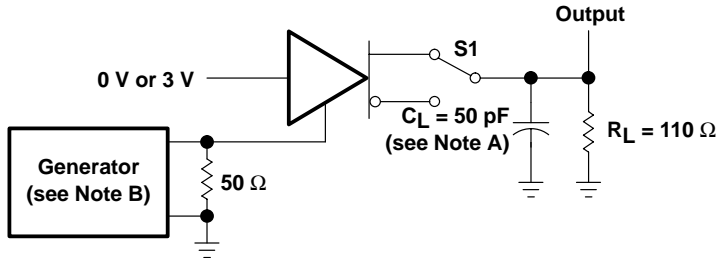
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\text{ MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ ,  $Z_0 = 50\ \Omega$ .

Figure 3. Driver Test Circuit and Voltage Waveforms

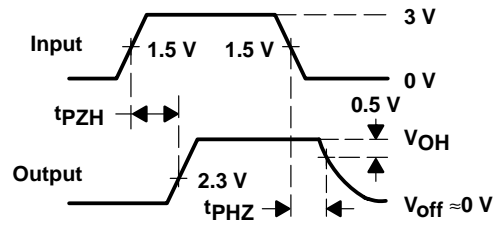
# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

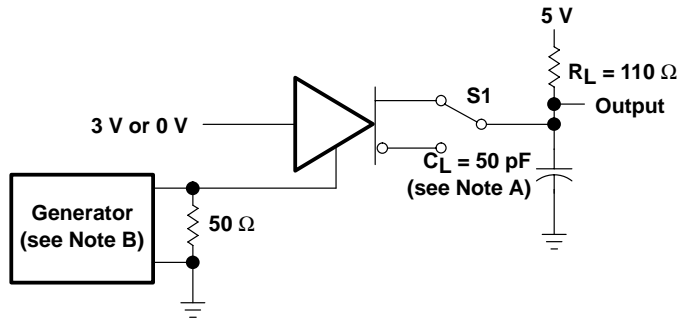


VOLTAGE WAVEFORMS

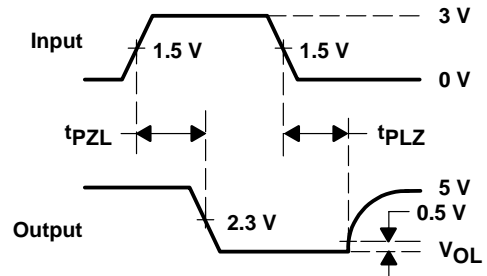
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

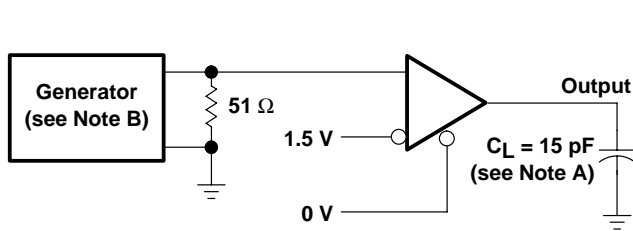


VOLTAGE WAVEFORMS

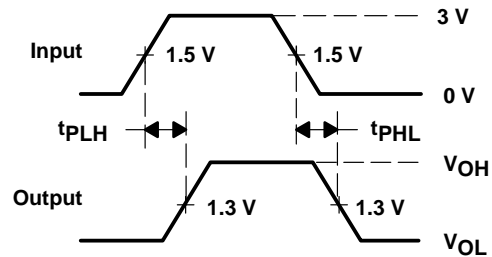
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 5. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

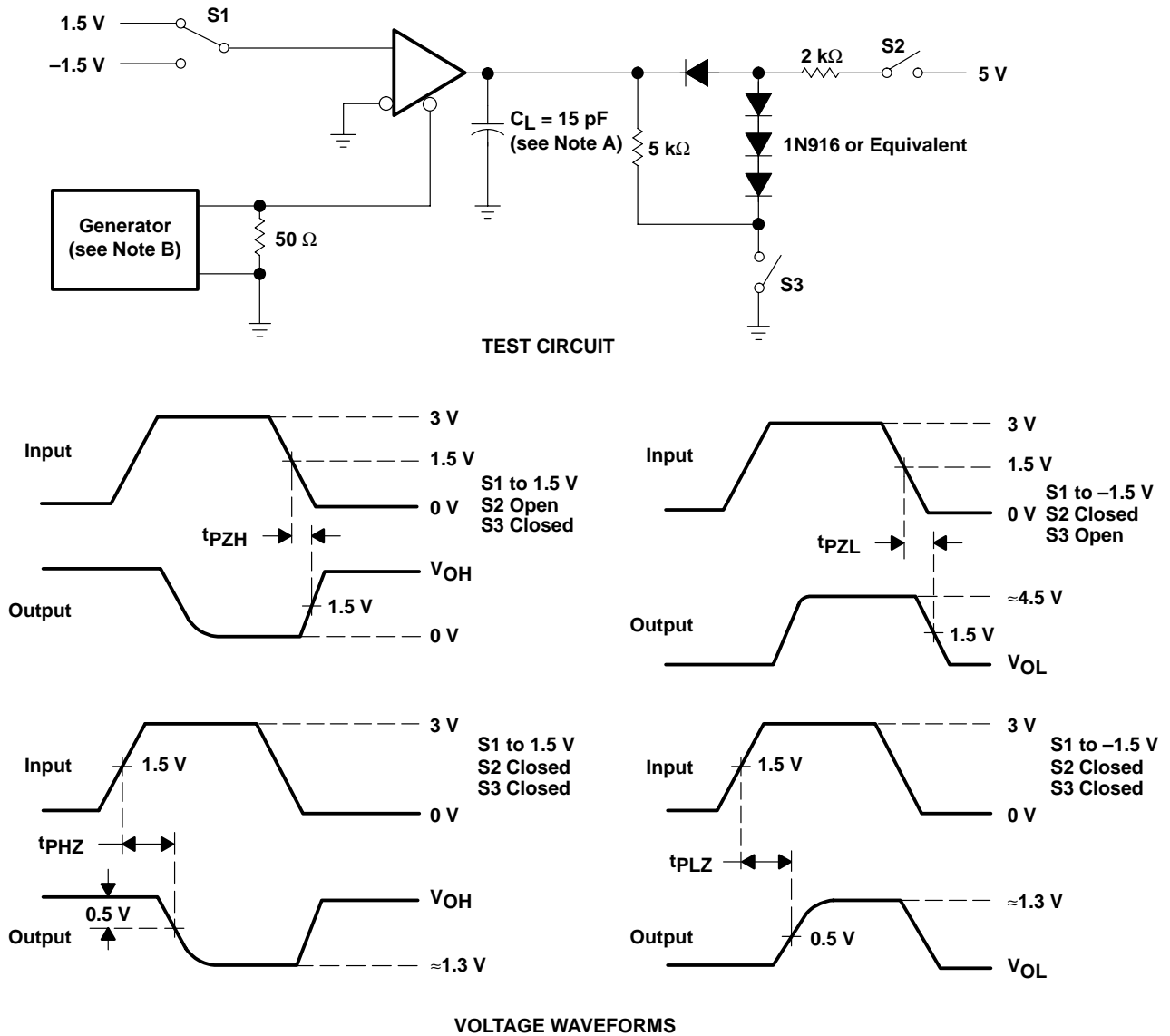
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 6. Receiver Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_0 = 50 \Omega$ .

Figure 7. Receiver Test Circuit and Voltage Waveforms

# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## TYPICAL CHARACTERISTICS

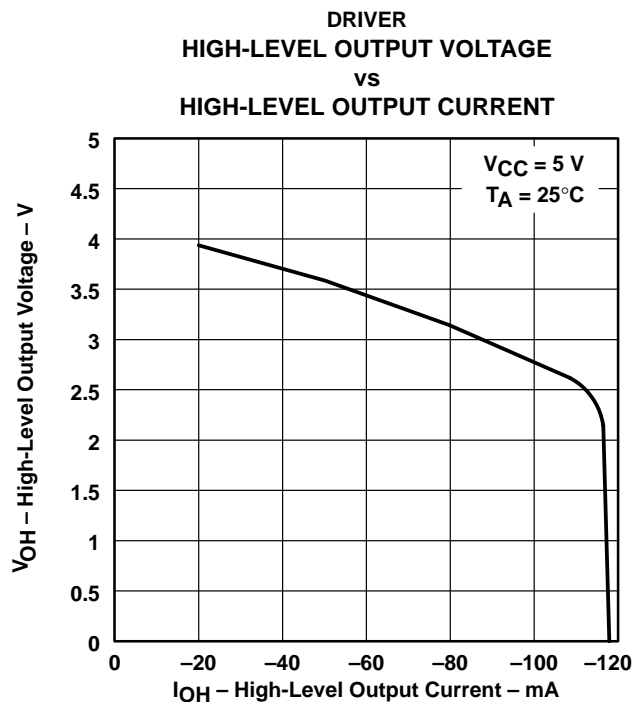


Figure 8

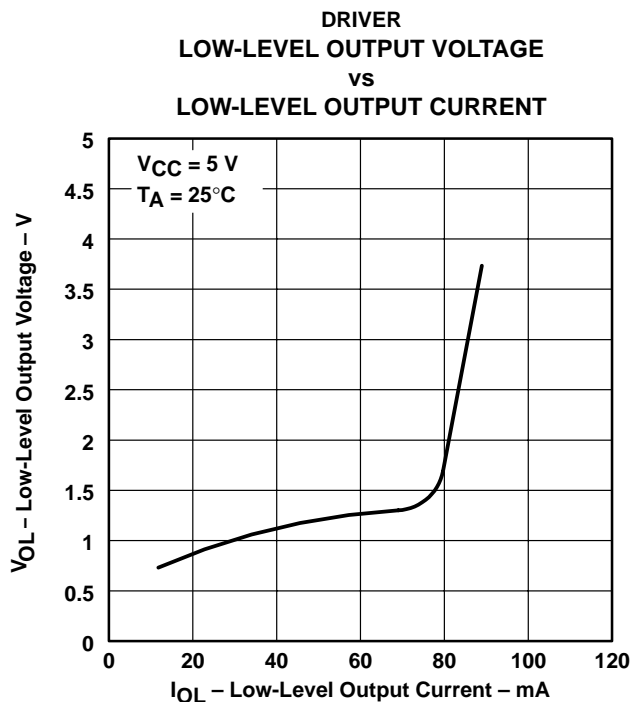


Figure 9

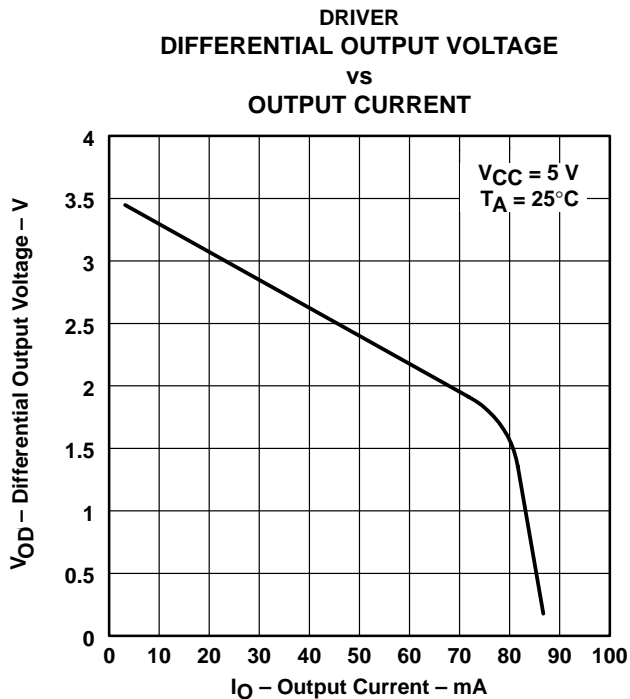
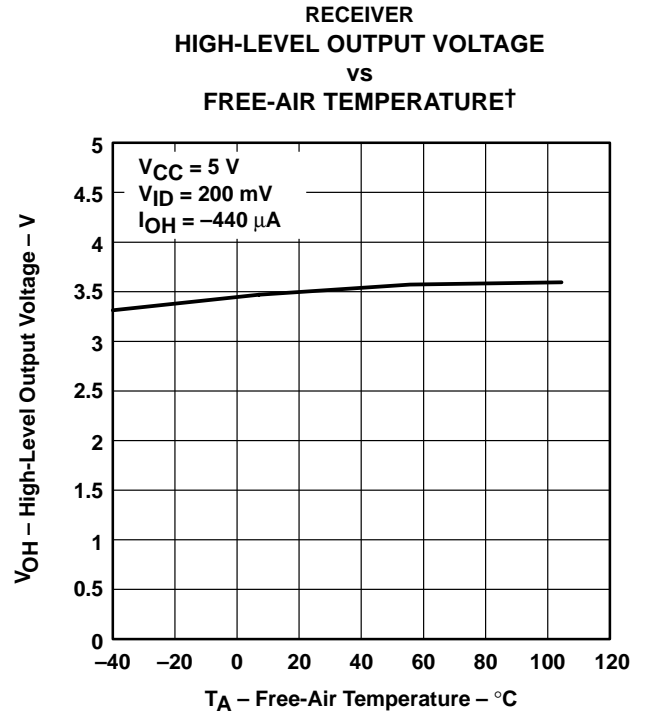
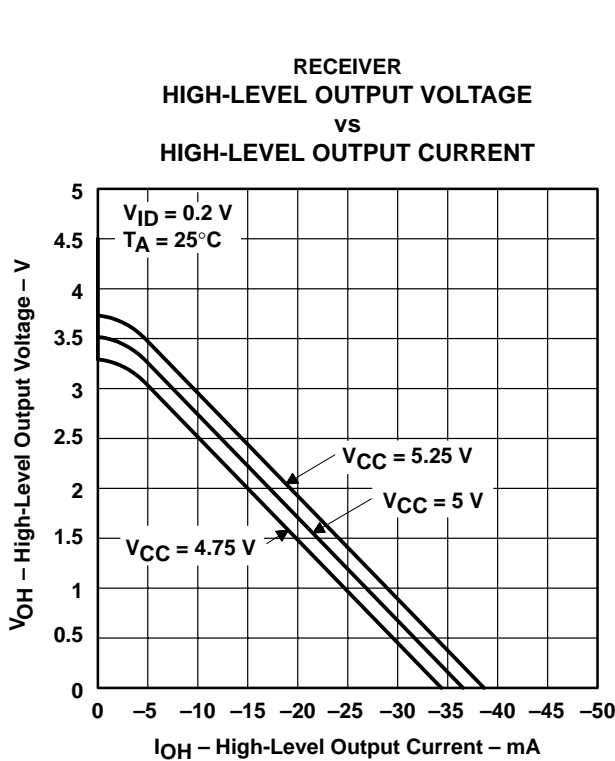


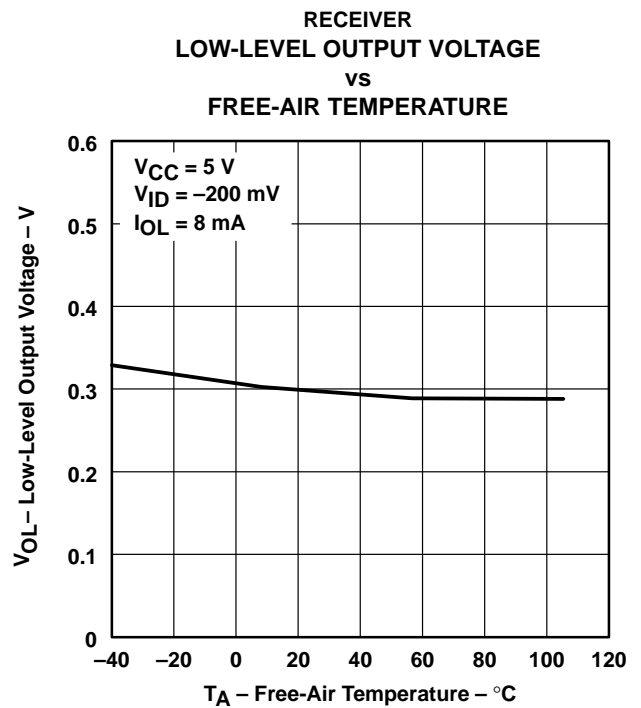
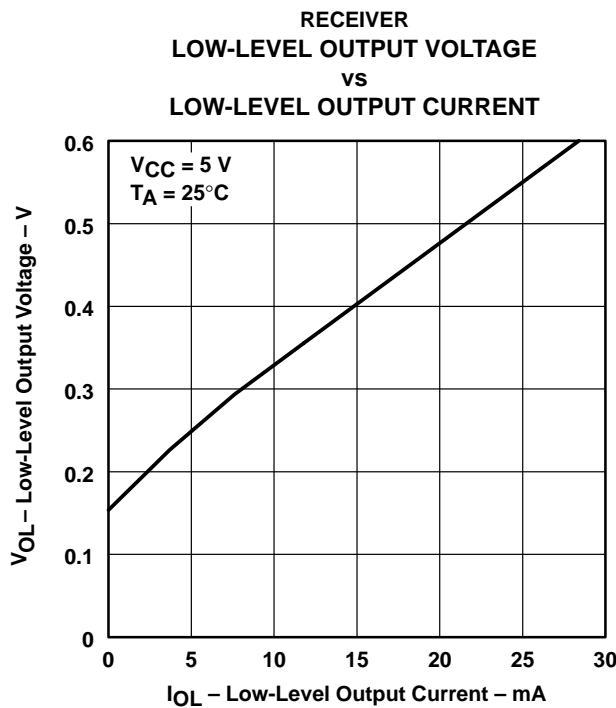
Figure 10



TYPICAL CHARACTERISTICS



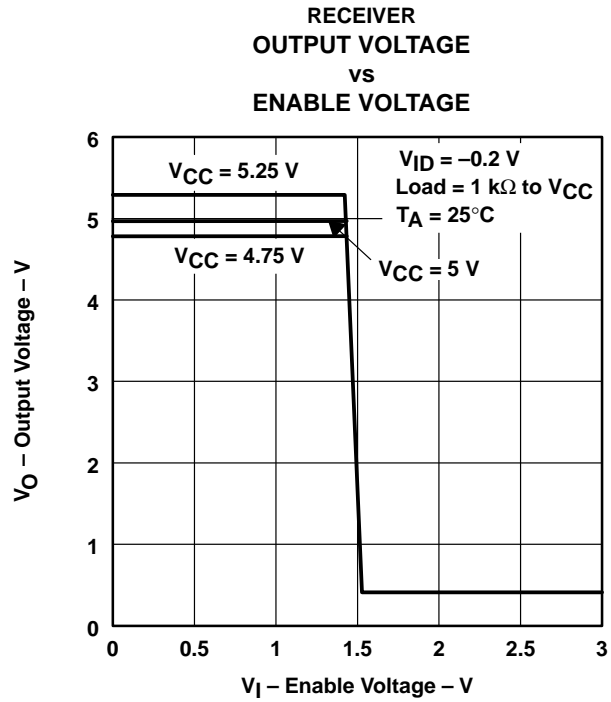
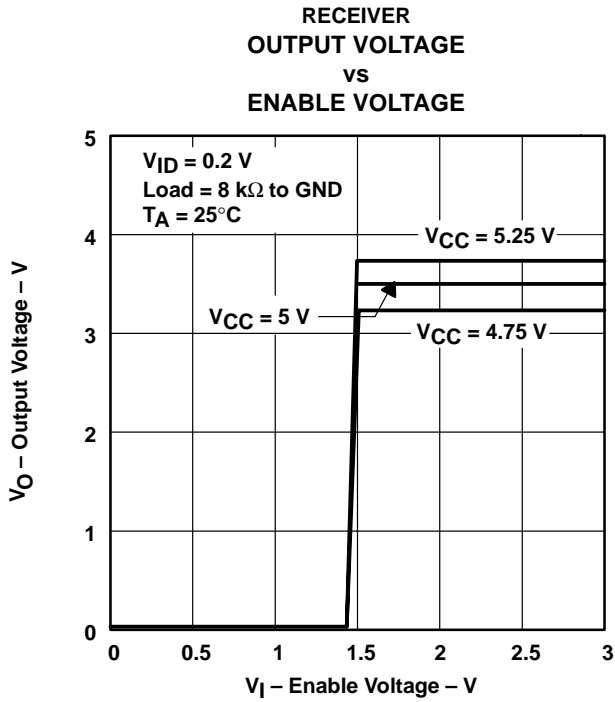
† Only the 0°C to 70°C portion of the curve applies to the SN75176B.



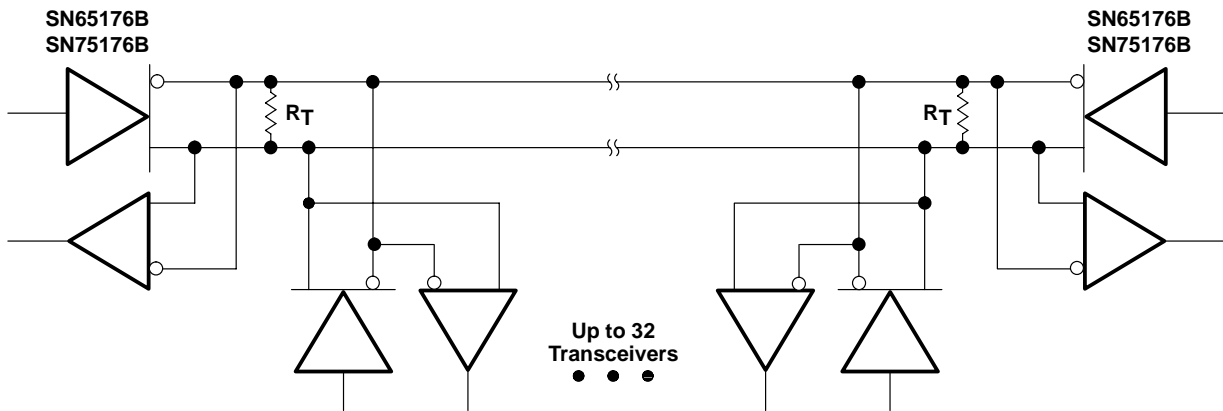
# SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS101D – JULY 1985 – REVISED APRIL 2003

## TYPICAL CHARACTERISTICS



## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 17. Typical Application Circuit**

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

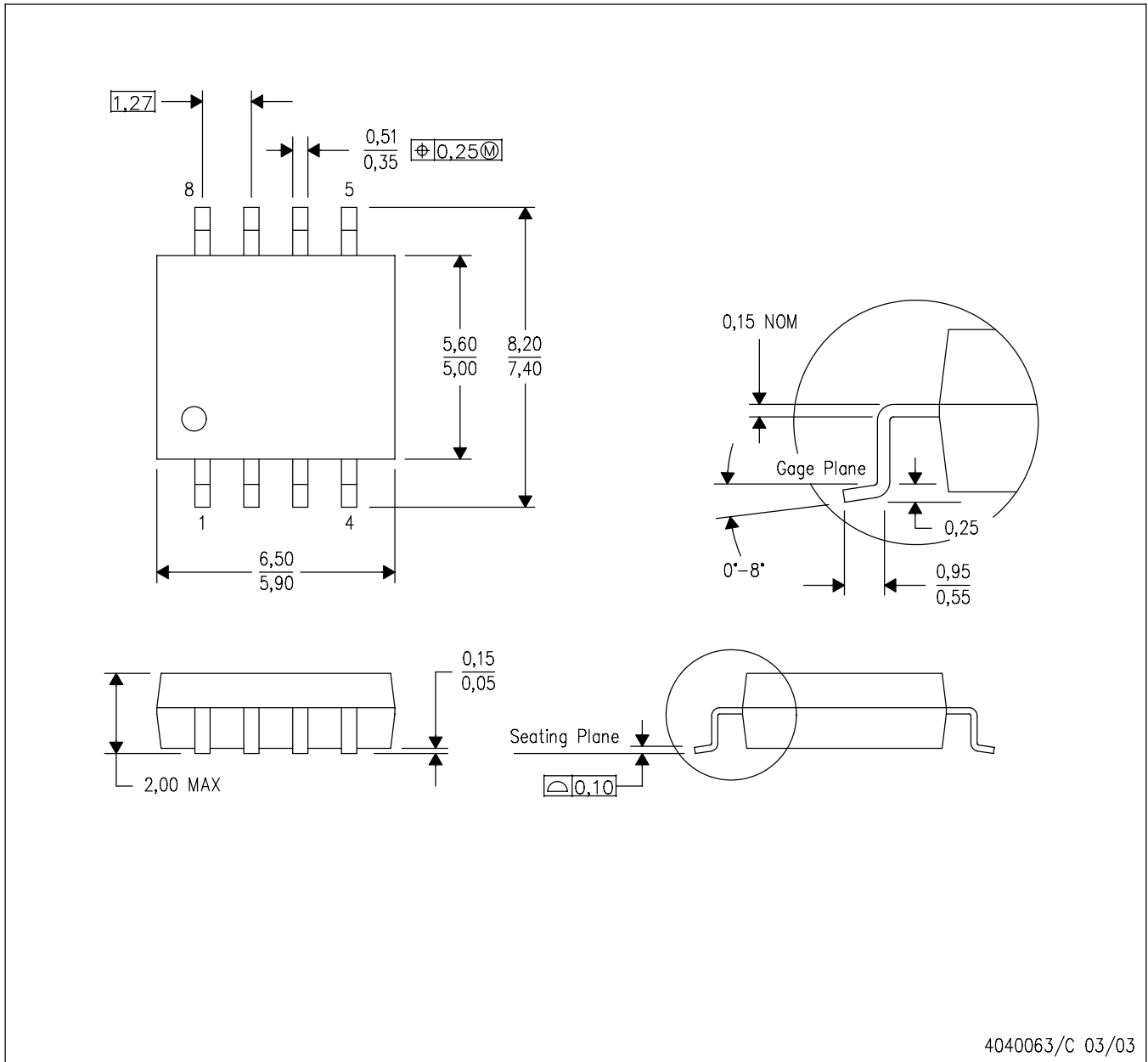


4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

PS (R-PDS0-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265